HARDWARE OF THE ORIGINAL IBM PC MICROCOMPUTER

12.1 Architecture of the Original IBM PC System Processor Board

12.2 System Processor Circuitry

12.3 Wait-State Logic and NMI Circuitry

12.4 Input/Output and Memory Chip-Select Circuitry

12.5 Memory Circuitry

12.6 Direct Memory Access Circuitry

12.7 Timer Circuitry

12.8 Input/Output Circuitry

12.9 Input/Output Channel Interface

PC memory map

PC system peripheral addresses
12.1 Architecture of the Original IBM PC System Processor Board

- 8255A I/O map

<table>
<thead>
<tr>
<th>Number</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Printer</td>
</tr>
<tr>
<td>1</td>
<td>Keyboard</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
</tr>
<tr>
<td>3</td>
<td>Asynchronous Communication (Secondary)</td>
</tr>
<tr>
<td>4</td>
<td>Asynchronous Communication (Primary)</td>
</tr>
<tr>
<td>5</td>
<td>Fixed disk</td>
</tr>
<tr>
<td>6</td>
<td>Diskette</td>
</tr>
<tr>
<td>7</td>
<td>Printer</td>
</tr>
</tbody>
</table>

12.2 System Processor Circuitry

- Clock generator circuitry
  - Clock generator circuitry serves three functions:
    - Clock signal generation
    - Reset signal generation (Power on reset)
    - Ready signal generation (Bus synchronization)
  - Three clock output signals of the 8284A:
    - The oscillator clock (OSC) at 14.31818 MHz
    - The TTL peripheral clock (PCLK) at 2.385 MHz
    - The 8088 microprocessor clock (CLK88) at 4.77 MHz
  - Clock generator circuitry provides synchronization of the 8088’s bus operations with its memory and I/O peripherals. For slow memory or peripherals, synchronization is achieved by inserting wait states into the bus cycle to extend its duration.
12.2 System Processor Circuitry

- Interrupt controller
  - External hardware interrupt interface is implemented for the IBM PC with the 8259A programmable interrupt controller.
  - The 8259A monitors the state of interrupt request lines IRQ0 through IRQ7 to determine if any external device is requesting service.
  - The operating configuration of the 8259A needs to be initialized at power-on of the system. This initialization is achieved by writing to the 8259A’s internal registers over the local bus.

12.3 Wait-State Logic and NMI Circuitry

- Wait-state logic circuitry
  - The wait-state circuitry is used to insert one wait state into I/O channel, I/O, and DMA bus cycles.
- Hold/hold acknowledge circuitry
  - The hold/hold acknowledge circuitry is used to grant the 8237A DMA controller access to the system bus.
- Nonmaskable interrupt circuitry
  - There are three sources for applying a nonmaskable interrupt to the 8088 microprocessor:
    - The 8087 numeric coprocessor (N P NPI)
    - The memory parity check (MPI)
    - The I/O channel check (PCK)

12.4 Input/Output and Memory Chip-Select Circuitry

- I/O chip select
  - The I/O chip select circuitry decodes the I/O address corresponding to the LSI peripheral devices, such as the DMA controller, interrupt controller, programmable interval timer, and programmable peripheral interface controller.
  - To access a register within one of the peripheral devices, an I/O instruction must be executed to read from or write to the register. The address output on address line A0 through A9 during the I/O bus cycle is used to both chip-select the peripheral device and select the appropriate register.
12.4 Input/Output and Memory Chip-Select Circuitry

Memory chip selects

- The output signals produced for ROM in the circuit are ROM address select (ROM ADDR SEL) and chip selects CS₀ through CS₇. The ROM ADDR SEL signal has two functions: to enable the ROM chip select decoder and to control the direction of data transfer through the ROM data bus transceiver.

<table>
<thead>
<tr>
<th>Address range</th>
<th>Chip select</th>
</tr>
</thead>
<tbody>
<tr>
<td>F0000-FFFFF</td>
<td>CS₀</td>
</tr>
<tr>
<td>F4000-F5FFF</td>
<td>CS₁</td>
</tr>
<tr>
<td>F6000-F7FFF</td>
<td>CS₂</td>
</tr>
<tr>
<td>F8000-F9FFF</td>
<td>CS₃</td>
</tr>
<tr>
<td>FA000-FBFFF</td>
<td>CS₄</td>
</tr>
<tr>
<td>FC000-FDFFF</td>
<td>CS₅</td>
</tr>
<tr>
<td>FE000-FFFFF</td>
<td>CS₆</td>
</tr>
</tbody>
</table>

12.4 Input/Output and Memory Chip-Select Circuitry

- The chip-select outputs used to control the operation of RAM are RAM ADDR SEL and ADDR SEL.
- The RAS₀, RAS₁, RAS₂, RAS₃ signals are used to refresh the DRAM devices in the RAM array.

<table>
<thead>
<tr>
<th>Address range</th>
<th>Active signal</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000-3FFFFF</td>
<td>RAM ADDR SEL</td>
<td>Inactive DACK 0 BRD</td>
</tr>
<tr>
<td>00000-3FFFFF</td>
<td>RAS₀, CAS₀</td>
<td>Active XMEMR or XMEMW</td>
</tr>
<tr>
<td>10000-1FFFFF</td>
<td>RAS₁, CAS₁</td>
<td>Active XMEMR or XMEMW</td>
</tr>
<tr>
<td>20000-2FFFFF</td>
<td>RAS₂, CAS₂</td>
<td>Active XMEMR or XMEMW</td>
</tr>
<tr>
<td>30000-3FFFFF</td>
<td>RAS₃, CAS₃</td>
<td>Active XMEMR or XMEMW</td>
</tr>
</tbody>
</table>

12.5 Memory Circuitry

ROM array circuitry

- The system processor board of the PC is equipped with 48Kbytes of ROM and either 64K or 256Kbytes of RAM.
- Each of the EPROMs is enabled by one of the ROM chip-select signals, CS₂ through CS₇, which are generated by the ROM address decoder.
- The address outputs on the lower 13 address lines of the system address bus, A₀ through A₁₂, are used to select the specific byte of data within an EPROM.
- The direction of data transfer through the data bus transceiver is set by the logic level at its data direction (DIR) input.

12.5 Memory Circuitry

RAM array circuitry

- In each RAM bank, eight 64K x 1-bit dynamic RAMs (DRAMs) are used for data storage, and ninth DRAM is included to hold parity bits for each of the 64K storage locations.
- The 74LS158 data selectors are used to multiplexed the 16-bit memory address into a byte-wide row address and byte-wide column address.
- Each DRAM device outputs a bit of data held in the storage location corresponding the selected row and column address. The byte of data is passed over data lines MD₀ through MD₇ to the 74LS245 bus transceiver.
- The parity generator/check circuitry is used to improve the reliability of data storage in the RAM array.
12.5 Memory Circuitry

- RAM array circuitry

RAM banks 2 and 3

12.6 Direct Memory Access Circuitry

- DMA circuitry
  - The DMA capability permits high-speed data transfers to take place between two sections of memory or an I/O device and memory.
  - There are 16 registers within the 8237A DMA controller that determine how and when the four DMA channels work. The 8088 communicates with these registers by executing I/O instructions.
  - DMA channel 0 is dedicated to RAM refresh and that channel 2 is used by the floppy disk subsystem.
  - Use of a DMA channel is initiated by a request from hardware (DRQ0 through DRQ3).

12.7 Timer Circuitry

- Programmable Interval Timer, PIT
  - Microprocessor interface and clock inputs
    - The timer circuitry controls four basic system functions:
      - Time-of-day clock
      - DRAM refresh
      - Speaker
      - Cassette
    - The programmable interval timer, 8253, provides three independent, programmable, 16-bit counters for use in the microcomputer system.
    - The control registers of the 8253 are located in the range 004016 through 004316 of the PC’s I/O address space.
    - 004016 -- Counter 0
    - 004116 -- Counter 1
    - 004216 -- Counter 2
    - 004316 -- Mode Control Register

- Outputs of the PIT
  - The 8253 output OUT1 is produced by timer 0 and is set at a regular time interval equal to 54.936 ms. This output is applied to the timer interrupt request input (IRQ0) of the 8259A interrupt controller, where it represents the time-of-day interrupt.
  - Timer output OUT2 is generated by timer 1 and also occurs at a regular interval of 15.12 μs. It is used to send request for service to the 8237A DMA controller and asks it to perform a refresh operation for the dynamic RAM subsystem.
  - The output OUT3 is generated by timer 2 and is used three ways in the PC:
    - It is sent as the signal T/22 OUT to port C of the 8255A PIC.
    - It is used as an enable signal for speaker data.
    - It is used to supply the record tone for the cassette interface.
12.8 Input/Output Circuitry

Three basic types of functions are performed through input/output circuitry:
- For 8088 to input data from the keyboard and output data to the cassette and speaker.
- The 8088 use this interface to read the setting of DIP switches to determine system configuration information.
- Certain I/O ports are used for special functions, such as clearing the parity check flip-flop and reading the state of the parity check flip-flop through software.

The I/O circuitry of the PC system processor board is designed using the 8255-A programmable peripheral interface (PPI) IC.

12.8 Input/Output Circuitry

The 8255A PPI has three 8-bit ports for implementing inputs or outputs. In the PC, ports PA and PC are configured to operate as inputs, and the port PB is set up to work as outputs.

- The ports PA, PB, and PC reside at the I/O addresses 0060H, 0061H, and 0062H, respectively.
- The operation of the 8255A ports are configurable under software control. Writing a configuration byte to the command/mode control register does this. The command/mode control register is located at address 0063H.

12.8 Input/Output Circuitry

8255A programmable peripheral interface

- The input port PA is used to both read the configuration switches of SW1 and communicate with the keyboard.
- Output port PB controls the cassette and speaker. It also supplies enable signals for RAM parity check, I/O channel check, and reading of the configuration switches or keyboard.
- The input port PC is used to read the I/O channel RAM switches (SW2), parity check signal, I/O channel check signal, terminal count status from timer 2, and cassette data.

12.8 Input/Output Circuitry

Inputting system configuration DIP switch settings

EXAMPLE
The system configuration byte read from input port PA is 7D16. Describe the PC configuration for these switch setting.

Solution:
Use the IN AL, 60H instruction to obtain the data from port PA.
Expressing the switch setting byte in binary form, we get
PA0PA1PA2PA3PA4PA5PA6PA7 = 7D16 = 011111012
We find that
PA0 = 1 indicates that the system has floppy-disk drive(s)
PA1 = 0 indicates that an 8087 is not installed
PA3PA2 = 11 indicates that the memory is 256K
PA5PA4 = 11 indicates a monochrome monitor
PA6PA7 = 01 indicates that the system has two floppy drives.

12.8 Input/Output Circuitry

Scanning the keyboard

The keyboard of the PC is interfaced to the 8088 through port PA of the 8255A.

The keyboard of the PC generates a keyspace code whenever one of its keys is depressed. Bits of the keyspace code are input to the system processor board in serial form at the KBD DATA pin of the keyboard connector synchronously with pulses at KBD CLK. The serial data is applied to the 74LS322 serial-in, parallel-out shift register.

In response to the IRQ1 interrupt request, the 8088 initiates a keyspace-code service routine. This routine reads the keyspace code by inputting the contents of the shift register.
12.8 Input/Output Circuitry

- Port C input and output functions
  - The five connected I/O channel RAM switches are used to identify the amount of read/write memory provided through the I/O channel. The settings of these switches are read through the 8255A PPI.
  - The four least significant bit lines of port PC indicate the status of the I/O channel RAM switches. The four most significant bit lines are supplied by signals generated else where on the system processor board. PC3 through PC7 allow the 8088 to read the state of the following signals through software:
    - RAM parity check (PC7)
    - I/O channel check (I/O CH CK)
    - Time terminal count (T/C2 OUT)
    - Cassette interface input (CASS DATA IN)

12.9 Input/Output Channel Interface

- The input/output channel is the system expansion bus of the IBM personal computer.
- The chassis of the PC has five 62-pin I/O channel card slots. Using these slots, special function adapter cards can be added to the system to expand its configuration.
- 62 signals are provided in each I/O channel slot:
  - 8-bit data bus
  - 20-bit address bus
  - Six interrupts
  - Memory and I/O read/write controls
  - Clock and timing signals
  - A channel check signal
  - Power and ground pins

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### 12.9 Input/Output Channel Interface

#### I/O channel interface

<table>
<thead>
<tr>
<th>Function</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address lines</td>
<td>A0-A19</td>
</tr>
<tr>
<td>Data lines</td>
<td>D0-D7</td>
</tr>
<tr>
<td>Address latch</td>
<td>ALE</td>
</tr>
<tr>
<td>Address enable</td>
<td>AEN</td>
</tr>
<tr>
<td>System clock</td>
<td>CLK</td>
</tr>
<tr>
<td>Memory write</td>
<td>MEMW</td>
</tr>
<tr>
<td>Memory read</td>
<td>MEMR</td>
</tr>
<tr>
<td>I/O write</td>
<td>IOW</td>
</tr>
<tr>
<td>I/O read</td>
<td>IOR</td>
</tr>
<tr>
<td>I/O channel ready</td>
<td>I/O CH RDY</td>
</tr>
<tr>
<td>I/O channel check</td>
<td>I/O CH CK</td>
</tr>
<tr>
<td>DMA request 1-3</td>
<td>DRQ1-DRQ3</td>
</tr>
<tr>
<td>DMA acknowledge 0-3</td>
<td>DACK0-DACK7</td>
</tr>
</tbody>
</table>

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#### I/O channel interface

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<tr>
<th>Function</th>
<th>Mnemonic</th>
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<tr>
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</tr>
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<td>ALE</td>
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</tr>
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<tr>
<td>Power and ground</td>
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